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As of November 20

December 2nd (Day-1)					
Highlight Session : Big Data					
	#	**Title**	**Author**	**Affiliation**	**Abstract**
13:30	**MC-O-66**	Development of robot fault detection system	YUSUKE MUKAE	Renesas Semiconductor Manufacturing	We have developed the detection system for quick trouble-shooting against robot faults because there are few systems for In-situ fault detection of transfer robots. As a way of the detection, we developed vibration monitoring device and pulse signal monitoring system. And we succeeded in detecting the robot faults by their combination. This paper reports on the detection system for robot faults by monitoring vibrations and pulse signal.
13:50	**MC-O-15**	Advanced Semiconductor Manufacturing Using Big Data	Tomio Tsuda	Panasonic	This paper describes development and actual utilization of a fab-wide FDC (fault detection and classification) for advanced semiconductor manufacturing using Big Data. In the fab-wide FDC, the collection of equipment's big data for the FDC judgment is required; hence we developed equipment monitoring system that handles the data in a superior method in high speed and in real time. We succeeded in stopping equipment and lots automatically in the equipment fault detection. In addition, we succeeded in development of the high-speed and high-accuracy process control system that implemented VM (Virtual Metrology) and the Run to Run function for the purpose to reduce process variation.
14:10	**PC-O-50**	Development of intelligent pad and application to analysis of pressure distribution on polishing pad in CMP process	Jaehong Park	Nitta Haas Incorporeted	Major polishing conditions such as pressure, velocity, temperature, pad surface asperity and slurry flow which determine the CMP performance, are not consistent during the polishing process. Conventionally, these parameters are detected by various monitoring methods in CMP polisher. Pad has been one of the important process factors from when the CMP process was applied to the semiconductor process. Pad is the media for adding pressure to wafer, for transforming slurry to wafer. In this study, we wanted to create added value to conventional pad as developing new functional pad.
14:50	**PC-O-20**	Modeling Abnormal Apparatus by Trouble-Based FDC	Hiroshi Matsushita	Toshiba	We performed trouble-based FDC to prevent recurrence of quality trouble. We have carried out multivariate analysis and classified the trouble by the number of sensors required for monitoring. Multivariate models are necessary for the majority of quality troubles.
15:10	**PC-O-68**	Understanding and Controlling Semiconductor Manufacturing Variability: A SEMATECH Mission	Bill W.Ross	SEMATECH	
15:50	**PO-O-2**	Pattern-independent PMD layer planarization by controlling its volume before CMP	Tomoyasu Kakegawa	SanDisk Limited	We achieved excellent planarization for a pre-metal dielectric (PMD) layer regardless of its pattern density distribution by making the distribution uniform before chemical mechanical polishing. The distribution control was done by lithography using a checkered mask on the high-density PMD area followed by etching of the PMD layer. After this planarization, the PMD height variation was approximately 8 nm (approx. 1% of PMD height) within chip, less than one-tenth variation compared with conventional planarization. The planarized PMD layer suppressed the defocusing in lithography for contact hole formation on the layer; thus, contact-open failures were drastically decreased in a chip of approx. 50 × 110nm in diameter and 620-nm-high contact holes. The number of defects were one-thousandth that of a conventionally planarized PMD layer.
16:10	**PO-O-17**	Failure measures for W-CMP process	Hiroshi Shibayama	Toshiba	We found a problem caused by slurry residue on a CMP polishing pad. This problem shortens the replacement cycle, and doubles the number of polishing pads used, consequently increasing the cost. However, the problem was solved by optimizing the CMP polishing conditions. This paper explains the solution in detail.
16:30	**YE-O-69**	Measurement and Control of Nanodefects in Liquids	Micheal Lercel	SEMATECH	

PO-1 & MS & MC & PE Session					
	#	Title	Author	Affiliation	Abstract
13:30	PO-O-36	Variability Improvement of Electrical Characteristics in MOSFETs with High-k HfON Gate Insulator by Si Surface Flattening	Shun-ichiro Ohmi	Tokyo Institute of Technology	Variability improvement of metal-oxide-semiconductor field-effect transisitors (MOSFETs) characteristics with high-K HfON gate insulator by Si surface flattening was investigated. The Si surface flattening process was carried out by Ar/4.9%H2 anneal utilizing rapid thermal annealing (RTA) system. The HfON gate insulator was formed by the in-situ Ar/O2 plasma oxidation of HfN utilizing electron cyclotron resonance (ECR) plasma sputtering. The Si surface flattening was found to significantly imporve the threshold voltage variability of MOSFET with HfON gate insulator for the first time. Furthermore, measurement temperature stablity was improved by introducing the Si surface flattening process.
13:50	PO-O-44	Effect of Plasma Process for Sidewall SiO2 film	Tatsuhiko Tanimura	Tokyo Electron	The physical and electrical characteristics of SiO2 treated by plasma oxidation on top and sidewall have been evaluated. The plasma process is less effective for SiO2 on sidewall compared with on top and further less for small pattern. The characteristics are sensitive to plasma condition in deposition sequence for sidewall while little as post treatment and for top. Species in plasma which little contribute to form SiO2 films can improve insulating properties.
14:10	PO-O-35	Investigation of metal residue on sidewall spacer in NiPt silicide process	Takashi Tonegawa	Renesas Semiconductor Manufacturing	In this paper, we report on the effect of NiPt silicide condition for metal residue removal on sidewall spacer. We found out that metal residue on silicon nitride spacer consisted mainly of Pt. Pt residue was significantly suppressed by SPM process time increase and low 1st RTA temperature.
14:50	MS-O-24	Measurement of vibration amplification characteristics of installed semiconductor equipment	Kaori KOMODA	Taisei Corporation	Seismic countermeasure for semiconductor equipment is very important. To consider the anti-seismic measure, we aimed to gain vibration amplification characteristics by simpler method, minute vibration measurement. The measurement was carried out on the exposure equipment with and without excitation on the floor near the equipment; consequently transfer function from the floor until the equipment was acquired as the equipment's vibration amplification characteristics. Additionally, it was implied that vibration amplification characteristics of semiconductor equipment help us estimate the movement of each part in the equipment when earthquake occurred and the information was useful to consider countermeasures against earthquakes.
15:10	MS-O-23	The Semiconductor Parts Refurbishment Operation Efficiency Optimization	Kai Lun Lin	UMC	The global warming problem has been getting worse than ever and the eco system is still suffering the pollution from the waste caused from the human beings. The way to reduce the carbon emissions is various, but the way to get the profit from the carbon emissions reduction is very rare. The profit of the cost saving could be about hundreds of millions dollars per year and our goal is trying to achieve both that above mentioned.
15:50	MC-O-3	Development of Wafer Transfer Simulator based on Cellular Automata	Hiroe Watanabe	TowerJazz Panasonic Semiconductor	This paper describes a homemade wafer transfer simulator based on cellular automata theory for such a complicated semiconductor multi-cluster tool. All the errors in the simulation became within only 30 seconds to the actual data. This theory is very simple and the simulator is made by a spreadsheet application, so anybody who has some knowledge of the application can develop it without equations. And in the modification process, it was unveiled that the multi-cluster tool in this paper had many logic failures on the wafer transfer system. The throughput will be improved by 6.9% if all the misunderstanding logics are removed.
16:10	MC-O-32	Daily Target Setting with Inclusion of Induced Variability	Yu-Ting Kao	National Taiwan University	In semiconductor manufacturing, the particles on the surface of chamber parts become an important issue, but conventional techniques such as wiping or using an air gun are insufficient. Therefore, we propose aerosol cleaning with liquid droplets as a technique to effectively remove particles on the surface. The number of particles on the surface of the chamber parts removed by aerosol cleaning with liquid droplets could be a single digit lower than that of the conventional technique. Additionally, it is possible that not only particles but also by-products were removed by aerosol cleaning with liquid droplets.
16:30	PE-O-62	An Actinic Blank Inspection tool for EUVL HVM	Hidehiro Watanabe	EUVL Infrastructure Development Center (EIDEC)	EIDEC and Lasertec Corp. develop an Actinic Blank Inspection tool to qualify the EUV mask blanks to be used in LSI high volume manufacturing with EUVL. The developing ABI tool has a capability to identify the location of captured multi layer defect accurate enough to mitigate the captured defect in the succeeding mask fabrication process steps, besides the tool has a sufficient defect detection capability in accordance with the lithographic requirement to avoid the impact on printing layout.

December 3rd (Day-2)

YE Session (Century A)

	#	Title	Author	Affiliation	Abstract
14:00	YE-O-9	Carrier Profiling Technology in 10 Nanometers Devices	Jun Hirota	Toshiba	The advanced carrier concentration evaluation scheme was proposed with combined higher precise SSRM measurement and TCAD analysis in this study. The CC method was applied to variation reduction of SSRM resistance to more accurately characterize for the device. The SSRM measurement of advanced flash memory was successfully demonstrated with adapted thesetechnologies. This result suggests strongly that 10 nm order size device can be measured by using SSRM with the CC method.
14:20	YE-O-37	Recoil Particle Elimination from Turbo Pump	Tsuyoshi Moriya	Tokyo Electron	We have verified the existence of recoil particles from turbo molecular pump. The recoil particles may be the root cause of yield degradation of vacuum processes such as plasma etch processes. To eliminate the recoil particles, they can be trapped inside the turbo molecular pump or in the manifold. We found that the particle trap improved the yield.
14:40	YE-O-27	Particles Transport in Etching Chamber with Coulomb Force	Masaki Ishiguro	Hitachi High-Technologies	Particle transport with Coulomb force was studied in both plasma (Ar/O2/N2) ON and OFF periods, which was done in microwave-electron cyclotron resonance plasma (M-ECR) etcher. The relationship between particle count attached on the wafer and wafer potential was researched, where wafer potential was supplied by RF bias and DC bias during plasma ON and OFF period respectively. In plasma ON period, particle counts decreased as the RF bias power increased. In plasma OFF period, particle counts decreased when wafer potential was set positive. These results enable us to understand particle charge negatively in plasma ON period and particle charge positively in plasma OFF period. In this study, we found controlling particle transport with Coulomb force by wafer potential is effective for particle attachment prevention.
15:00	YE-O-16	Yield Enhancement in MEMS Wafer Level Fabrication by Whole Process PLS Model	Masaki Kitazawa	OMRON	This paper presents a real example of data-based yield enhancement. In 3DIC and MEMS fabrication, it is hard to identify a key process for product quality by analyzing each process separately, and the efficient analysis based on operation data of whole manufacturing process is required. To enhance the yield, we built a PLS model with gathered whole process data, and identified a key process. Next, we experimented for yield enhancement. We tuned a condition of the identified process, and successfully controlled product quality for yield enhancement. The experimental results suggest that the modeling with whole process data is effective to identify a key process and control product quality.
15:40	YE-O-57	Impact of Root Cause" Identification of Parametric Failure by Using Equipment Data in CMOS Image Sensor"	Masaaki Fujii	TowerJazz Panasonic	
16:00	YE-O-51	Voltage Contrast Detection for Challenge Systematic Killer Defects on Advanced High Voltage and CMOS Image Sensor Device	Ying-Hsun Chen	TSMC	Electron-beam inspection (EBI) was developing to enhance monitoring the challenge contact leakages defects for the advanced special devices. For 55nm high voltage (HV) device, Inter-layer dielectric (ILD) gap filling is challenged and can be caught by negative mode EBI as dark voltage contrast (DVC) defect. The DVC defect counts were improved with reducing ILD deposition/sputtering (D/S) ratio. For 65nm CMOS image sensor (CIS), contact-to-poly (CT/poly) leakage also can be enhanced with negative mode EBI. The DVC count was correlative to the contact CD (Critical Dimension) size and CT/poly overlay. Negative mode EBI was effective monitor methodology to optimize the process window for the advanced special devices.
16:20	YE-O-61	Impact of Plasma Induced Charging from Implanter and ESC Dechuck process in wafer Fabrication	ANG GHIM BOON	Global Foundries	Plasma induced Charging has always resulted in different level of damages and impacted the wafer yield to different extent in wafer Fabrication. Understanding multiple causes of charging resulted from equipment of different wafer processes either through vendor or “real” case studies will always benefit engineers from yield enhancement, Process Integration, process and equipment to resolve the encountered issues more quickly. This paper has specifically provided two detailed illustrated cases to emphasis on the impact of charging in implanter as well as Etch. For the implanter charging, the defect site occurred only on the large N+ poly/NWELL varactor in which the causes were due to insufficient electrons to neutralize the positive Ion Beam resulting in charging as a result of Disk and Bias Aperture poor grounding as well as Bias Aperture Assembly alignment out of position. For the Etch charging issue, it was due to discharge of charges from ESC chuck to substrate during wafer de-chuck on those unipolar standard de-chuck process with higher RF lifetime. It serves as a good reference to other wafer Fabs encountering such an issue.
16:40	YE-O-40	Scan Chain Design-Based Defect Inspection Approach for Faster Scan Chain Yield Ramp	Goh Szu Huat	Global Foundries	In today’s competitive electronics industry where profit margin favours faster product time-to-market, there is a need to accelerate product yield ramp. In modern scan-based integrated circuits, high scan chain yield is pivotal to overall product yield ramp. For scan chain failure fault isolation, structural test followed by chain diagnosis is commonly used to narrow down the suspected failure causation. However, the device is required to be fully fabricated and testable before any debug can occur. In this paper, we propose an innovative methodology which enables defect on scan chains to be detected as early as the inception of device fabrication for quicker process improvement feedback. Scan cells and nets information extracted from design data file are used to guide and optimize defect inspection at critical process steps. The success of such methodology is proven experimentally on a 20nm technology testchip. Metallization defects causing scan chain failures, which is impossible to be detected inline traditionally, can be realized. The results also demonstrate the potential to shorten logic yield learning based on scan chain defects from months to weeks.

PC session / PO-2 Session (Century B)					
	#	Title	Author	Affiliation	Abstract
14:00	PC-O-25	Correlational study between SiN etch rate and plasma impedance in electron cyclotron resonance plasma etcher for advanced process control	Takeshi Ohmori	Hitachi	The correlation between the change in the etching rate of SiN and the change in the monitored plasma impedance was investigated to estimate the capability of CD prediction with a PIM. The results obtained with the PIM were compared with those of OES, which was performed using the emission intensity ratio of C2/H, and showed that the SiN etching rate is strongly correlated with several values obtained with the PIM. We conclude that the PIM has the potential to predict CDs with the same accuracy as that of OES.
14:20	PC-O-30	Enhancement of Virtual Metrology Performance for Plasma-Aided Processes by Using Process Plasma Monitoring	Seolhye Park	Seoul National University	Virtual Metrology (VM) for C4F8 plasma-aided oxide etching processes is developed to predict and monitor the process results such as an etching rate with improved performance. For FDC and APC, high performance of VM is certainly required and PCR(Principal Component Regression) is preferred technique for VM despite this method requires many number of data set to obtain guaranteed accuracy. By the adoption of plasma monitoring parameters as PCs,information about the reactions in the plasma volume, surface, and sheath property is included into the PCR; thus, the performance of VM is secured even for insufficient data set provided cases.
14:40	PC-O-39	Use of Traditional Approaches in the Three-dimensional Integrated Circuit TSV Package Failure Analysis	Hao TAN	Global Foundries	Three-dimensional integrated circuit (3D IC) chips using through-silicon via (TSV) have caused many reliability challenges compared with normal 2D IC microchips. Therefore, electrical testing (ET) is the critical measurement for both process monitoring and package structural integrity analysis. Consequently, failure analysis (FA) on such ETs plays a vital role for process and yield improvement. In this paper, traditional FA approaches such as micro-probing and thermal analysis were successfully applied to ET FA cases in two prototype 3D TSV package units, proving the effectiveness of both techniques in the 3D IC FA.
15:00	PC-O-21	Defect Classification Solution for 1X nm DR using an Unpatterned Wafer Inspection System	Xugang (Jack) Yan	KLA-Tencor	
15:40	PO-O-12	Optimization Method for CVD Chamber Cleaning	Masayuki Takata	Toshiba	The plasma CVD's chamber cleaning process needs excellent particle performance to achieve high production yield, and so the optimization of the cleaning condition is very important. This paper proposes a method of optimizing the cleaning condition without using expensive equipment. It involves deconvoluting the peak of exhaust line pressure obtained from the equipment and optimizing each peak. We checked particle counts during a short running test while using the cleaning condition determined by the method. As a result, no increase of particle counts was detected and the particle counts were not dependent on deposition count in the chamber in this test.
16:00	PO-O-19	Defect reduction by reducing wafer charging	Tomohisa Satoh	Toshiba	Reduction of the electric charge on a wafer is proposed to decrease defects attributable to particles. In the plasma etch process, small particles adhere to a wafer and cause defects. We have investigated the relationship between the electric charge on a wafer and the number of defects. It has been found that the electric charge decreases when radio frequency (RF) power is reduced or the process time is shortened. The number of defects decreases when the electric charge is reduced.
16:20	PO-O-42	negative-tone imaging process and materials with EUV exposure	Toru Fujimori	EUVL Infrastructure Development Center (EIDEC)	Negative-tone imaging (NTI, using organic solvent based developer) with EUV exposure (EUV-NTI) has advantages for line-width roughness (LWR) due to their dissolution behavior, like low swelling and dissolving smoothly. Novel chemical amplified resist materials for EUV-NTI have been studied to improve LWR and sensitivity. Also, process conditions of EUV-NTI are very effective describes the recent progress of EUV-NTI.
16:40	PO-O-46	A Theoretical Modeling of Rate Enhancer for Si CMP	Akira Endou	FUJIMI INCORPORATED	A theoretical modeling of rate enhancers for Si CMP processes is of paramount importance in the design of more effective slurries. In this study, the possible factors related to the removal rates for Si were studied by means of computational chemistry methods. It was found that some chemical agents possess the ability to weaken Si-Si bonds due to the interaction with the Si(100) surface. The ratios of the model removal rates for Si were also calculated by combining the published CMP model and the present results derived by computational chemistry methods, which agreed with the experimental results.

Interactive Poster Session					
	#	Title	Author	Affiliation	Abstract
	MS-P-13	Analytical Approach for Semiconductor Production Line Control	Shigeta Kuninobu	Toshiba	In this paper, we propose approximations for throughput (ϕ(k)) and TAT (T(k)) for m-tandem G/G/(s)/(k) waiting queque, representing semiconductor production line (Figure 1). A lot is kept waiting before the production line if |WIP| =k where |WIP| is the number of WIP and k is the max number of WIP in the production line. We can determine optimal k by using ϕ(k) and T(k), on that increasing k makes throughput higher but makes TAT longer and vice versa.
	PE-P-34	Robustness improvement of inline optical metrology system	Hideaki Abe	Toshiba	– For improving measurement uncertainty of optical metrology, the concept of horistic robust metrology with more accurate inline metrology tool and inline reference metrology tool with high frequency is proposed. Three features which are inline metrology tool with multiple measurement, inline reference metrology tool and total metrology checking system can reduce measurement robustness error. Multi measurement system such as multi azimuth metrology can reduce the impact on parameter correlation and improve measurement robustness for unpredictable shape changing. GI-SAXS has high capability of measurement robustness for under-layer structure changes because GI-SAXS uses total reflection signal with very short wavelength. Inline reference metrology system “VMS” is combined inline metrology tools and non-destructive reference metrology tools. VMS can detect the false alarm error and the not-detectable error caused by measurement robustness decay of inline metrology tools. VMS, which is composed of multi measurement system such as multi azimuth metrology and inline reference tool such as GI-SAXS, has a potential to detect metrology system errors caused by unpredictable process.
	PO-P-10	Method to achieve high selectivity and precise etching uniformity control for gas phase etching system	E.W.Chiu	TSMC	In this study, a method to achieve high etching selectivity and precise etching uniformity control for a gas phase etching system is demonstrated. Multi-cycle etching can achieve highly selective etching by incubation time difference on various films and wafer angle control between multi-cycle etching steps can realise precise etching uniformity control by improving etching uniformity which seems to come from gas flow distribution. This multi-cycle etching method with wafer angle control significantly contributes to not only high selectivity but also margin enhancement within a tight uniformity specification and leads to productivity benefits through downtime reduction.
	PO-P-48	EUVL resist pattern formation analysis during development; in situ analysis using HS-AFM	Motoharu Shichiri	EUVL Infrastructure	
	YE-P-26	Yield prediction method of product with a redundant circuit	Hideki Yasui	Toshiba	In conventional yield prediction method, accurate yield prediction of product with a redundant circuit is difficult. Thus, yield improvement of the most advanced chips was not done efficiently. Therefore, we propose new yield prediction method and become able to predict yield improvement of product with a redundant circuit accurately.
	YE-P-53	The new method developed by the correlation method of monitoring minute particles in space	Ryunosuke Arita	Kumamoto University	It is the purpose of the new air flow detection method developed in the clean room in this study. Air flow is detected using a xenon flash lamp capable of irradiating a large area. It would help to solve the problems caused by particles present in the clean room by the air flow detection. I showed the effectiveness of the air flow detection method based on correlation method in this paper.
	YE-P-70	A Study of Photovoltaic Electrochemical and Galvanic Effect from CMP and Clean process on Semiconductor process yield	Chen Changqing	Global Foundries	As the semiconductor technology keeps scale-down, the semiconductor structures become more and more sensitive to the uniformity of the process parameters. Normally, the composition concentration and ration are very important in the wet process, while the potential uniformity was not noticed and highlighted in the process control of wet process. But in this paper, in-depth investigation and study of potential uniformity impact on wafer yield was conducted. As known to all, light and temperature usually was the source or external stimulus of the potential variation within the wafer in wet process. So the light and temperature control are also very important in wet process based on our study. In this paper, both temperature and light impact on the wet process, CMP and clean process were studied, and in-depth mechanism of light and temperature effect was built up.

	#	Title	Author	Affiliation	Abstract
	UC-P-29	Particle Reduction by Controlling Wafer Voltages in Vacuum Transfer Chamber	Tomoyuki Tamura	Hitachi High-Technologies	The effect of a wafer voltage on charged particle attachment onto the wafer in vacuum wafer transfer chamber in etch system was studied. A simulated result showed that a wafer voltage should be reduced to few volts to avoid charged particle attachment. We studied a method of reduction of wafer voltage and found that electrostatic capacitance of wafer placed on the transfer hand should be optimized instead of neutralizing remaining charges on the wafer. A newly developed conductive robot hand was installed in our etching system and it successfully reduced wafer voltage and particle attachment in a vacuum wafer transfer chamber.
	UC-P-45	Effective proposal for the resist outgassing test on the EUV lithography	Isamu Takagi	EUVL Infrastructure Development Center (EIDEC)	Witness-sample testing is the standard method for evaluating the potential for extreme ultraviolet (EUV) optics contamination by resist outgassing. Resists are expected to be correctly qualified using this method before they are used in high volume manufacturing exposure tools. However, the present capacity of outgassing test facilities is insufficient for anticipated needs, based on the current capacity of existing EUV exposure tools. This paper defines an enhanced “resist family” concept for reducing the required number of outgassing tests. The relationship between outgassing and the protecting group of the base resin is discussed according to results obtained with model resists.
	UC-P-18	Particle removal force measurement from the Si substrate by atomic force microscopy	Shigeru Kawamura	Tokyo Electron	Particle removal forces from the Si substrate are important for the development of the cleaning process to remove the particles on the Si. T.-G.Kim.[1] reported the removal forces of 100nm and larger particles on Si substrate.In this paper, the forces were measured by using atomic force microscope(AFM) and dependence of the size ranging from 20nm to 373nm were analyzed from frictional signal of AFM. Removal forces are proportional to the radius of the particle. Therefore, the removal forces depends on the contact areas of the each spherical particle due to the adhesive force between particles and substrate. Furthermore,these particle removal forces are sufficiently smaller than the force of the Poly-Si pattern collapse.
	UC-P-38	Aerosol Cleaning with liquid droplets for super fine surface on chamber parts	Hidefumi Matsui	Tokyo Electron	In semiconductor manufacturing, the particles on the surface of chamber parts become an important issue, but conventional techniques such as wiping or using an air gun are insufficient. Therefore, we propose aerosol cleaning with liquid droplets as a technique to effectively remove particles on the surface. The number of particles on the surface of the chamber parts removed by aerosol cleaning with liquid droplets could be a single digit lower than that of the conventional technique. Additionally, it is possible that not only particles but also by-products were removed by aerosol cleaning with liquid droplets.
	PC-P-8	Practical and high-speed load impedance monitoring system for anomaly detection in plasma processing	Yuji Kasashima	National Institute of Advanced Industrial Science and Technology(AIST)	A high-speed and practical load impedance monitoring system is successfully developed. The detection system measures forward and reflected rf powers, including phase information, simultaneously with capacitances of variable capacitors, which allows real-time monitoring of load impedance. The results of this study demonstrate that the system can detect micro-arc discharges and wafer movements at high speed and high sensitivity from a 50Ω transmission line, and reveal that a significant change in load impedance is caused by these anomalies. This method is expected to contribute to improvements in plasma processing, production yield, and overall equipment effectiveness in semiconductor manufacturing.
	PC-P-63	Performance of VM Models Based on PCR and Sensitivity Test for Oxide Etch Process in triple frequency CCP	Yunchang Jang	Seoul National University	The selection rule of variables is essential part for the accuracy and reliability of the Virtual Metrology (VM) model. In this study, as the variation selection methods, principal component analysis (PCA), which is the statistical dimension reduction method, and the sensitivity raking test (SRT) method of variables are compared for the development of oxide etch process VM. The SRT based VM model has shown better performance than the PCA based VM in this data set, while the PCA based VM has higher applicability for the practical-mass production. These results imply that the importance of proper selection of VM models.
	PC-P-55	Secure Remote Connectivity and Big Data	Stuart Perry	ILS Technology	